

ABSTRACT OF THE DISCLOSURE

The present invention relates to address generation and in particular to address  
5 generation in a data processing apparatus. A data processing apparatus is disclosed.  
The data processing apparatus comprises: a processor core operable to process a  
sequence of instructions, the processor core having a plurality of pipeline stages, one of  
the plurality of pipeline stages being an address generation stage operable to generate an  
address associated with an instruction for subsequent processing by the pipeline stages,  
10 the instruction being one from a first group of instructions or a second group of  
instructions. The address generation stage comprises: address generation logic operable  
to receive operands associated with the instruction, to generate a shifted operand from  
one of the operands, and to add together, in dependence on the instruction, selected of  
the operands and the shifted operand to generate the address for subsequent processing  
15 by the pipeline stages; and operand routing logic operable, in dependence on the  
instruction, to route operands associated with instructions from the first group of  
instructions to the address generation logic and to route operands associated with  
instructions from the second group of instructions via operand manipulation logic for  
manipulation of the operands prior to routing to the address generation logic.  
20 Accordingly, addition instructions as well as a shift instruction are processed more  
quickly than other instructions. Because the addition instructions and the shift  
instruction occur more frequently than the other instructions, the overall performance  
of the pipeline is significantly improved.

25 (Figure 6A)